Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

1. (Currently Amended) A bandgap reference circuit comprising:

first, second and third current sources (CS1, CS2, and CS3) adjusted to have the same current, the first current source feeding into a first BJT device module (Q1), the second current source feeding into a second BJT device module (Q2) through a first resistor (R1), and the third current source connecting to a grounding voltage supply through a second resistor (R2);

a current summing circuit;

a first voltage passing unit connecting an output of [[CS1]] the first current source as its input and connecting its output to a first end of a third resistor (R3) and a first output of the current summing circuit;

a second voltage passing unit connecting an output of [[CS3]] the third current source as its input and feeding its output to a first end of a fourth resistor (R4) and a second output of the current summing circuit;

a fifth resistor (R5) connecting to a third output of the current summing circuit on a first end and the grounding voltage supply on a second end thereof,

wherein a first current through the fifth resistor [[R5]] bears a substantially linear relationship with a summation of a second current through the third resistor [[R3]] and a third current through the fourth resistor [[R4]],

wherein the outputs of the first and second voltage passing units track their respective inputs, and

wherein by selecting predetermined values for the first, second, third, fourth, and fifth resistors ~~R1, R2, R3, R4, and R5~~ in conjunction with selections of the first BJT device module [[Q1]] and [[Q2]] the second BJT device module, a reference voltage of the circuit across R5 the fifth resistor is independent of temperature variations.

2. (Currently Amended) The circuit of claim 1 further comprises an operational amplifier with its positive input connected to the output of the first current source [[CS1]] and negative input connected with the output of the second current source [[CS2]].

3. (Currently Amended) The circuit of claim 1 wherein the current summing circuit provides the first current through [[R5]] the fifth resistor equal to the summation of the second and third currents through the third resistor [[R3]] and the fourth resistor [[R4]].

4. (Currently Amended) The circuit of claim 1 wherein the second BJT device module [[Q2]] has a predetermined number of BJT transistors connected in parallel.

5. (Original) The circuit of claim 1 wherein the reference voltage is less than or equal to about 1V.

6. (Original) The circuit of claim 1 wherein a supply voltage of the circuit is less than about 1V.

7. (Currently Amended) The circuit of claim 1 wherein the first BJT device module [[Q1]] is a pnp type and receives the output of the first current source [[CS1]] at its emitter, and wherein [[Q2]] the second BJT device module is a pnp type and receives the output of the second current source [[CS2]] at its emitter through the first resistor [[R1]].

8. (Currently Amended) The circuit of claim 7 wherein a predetermined relationship among an emitter voltage of Q1 (V_{be1}) and an emitter voltage of Q2 (V_{be2}) may be expressed mathematically by ~~and the resistors~~ $(R5 / R3) * dV_{be1}/dT + ((R2 * R5) /(R1 * R4)) * d(V_{be1} - V_{be2})/dT=0$ ~~is zero~~, wherein dV_{be1}/dT and $d(V_{be1} - V_{be2})/dT$ are respective changes of the emitter voltage of [[Q1]] the first BJT device module and a difference

between the emitter voltages of the first and second BJT device modules ~~Q1 and Q2~~ with respect to temperature.

9. (Currently Amended) The circuit of claim 1 wherein ~~Q1 and Q2~~ the first and second BJT device modules have their collectors grounded so that the reference voltage (V_{REF}), an emitter voltage of Q1 (V_{be1}), an emitter voltage of Q2 (V_{be2}), and the resistors bear a predetermined relationship as represented mathematically by $V_{REF} = V_{be1} * (R5 / R3) + (V_{be1} - V_{be2}) * ((R2 * R5) /(R1 * R4))$.

10. (Original) The circuit of claim 1 wherein the first and second voltage passing units are unit gain buffers.

11. (Currently Amended) A bandgap reference circuit comprising:

first, second and third current sources (CS1, CS2, and CS3) with an output of the first current source [[CS1]] output feeding into a first BJT device module (Q1), an output of [[CS2]] the second current source feeding into a second BJT device module (Q2) through a first resister (R1), and an output of the third current source [[CS3]] connecting to a grounding voltage supply through a second resister (R2);

a current summing circuit for providing three current paths to the grounding voltage supply through third, fourth and fifth ~~three~~ resistors (R3, R4, and R5) respectively,

wherein the outputs of the first current source [[CS1]] and [[CS3]] the third current source are buffered and connected to the grounding voltage supply through [[R3]] the third and [[R4]] fourth resistors respectively,

wherein a temperature independent reference voltage (V_{REF}) across [[R5]] the fifth resistor is generated when an emitter voltage of Q1 (V_{be1}), an emitter voltage of Q2 (V_{be2}), and the resistors bear a predetermined relationship as represented mathematically by $(R5 / R3) * dV_{be1}/dT + ((R2 * R5) /(R1 * R4)) * d(V_{be1} - V_{be2})/dT = 0$, wherein dV_{be1}/dT and $d(V_{be1} - V_{be2})/dT$ are respective changes of the emitter voltage of [[Q1]] the first BJT device module and a difference between the emitter voltages of the

first BJT device module [[Q1]] and the second BJT device module [[Q2]] with respect to temperature.

12. (Currently Amended) The circuit of claim 11 further ~~comprises~~ comprising an operational amplifier with its positive input connected to the output of the first current source [[CS1]] and negative input connected with the output of the second current source [[CS2]].

13. (Currently Amended) The circuit of claim 11 wherein the current summing circuit provides the current through the fifth resistor [[R5]] to be proportional to the summation of the currents through the third resistor [[R3]] and the fourth resistor [[R4]].

14. (Currently Amended) The circuit of claim 11 wherein the second BJT device module [[Q2]] has a predetermined number of BJT transistors similar to [[Q1]] the first BJT device module connected in parallel.

15. (Original) The circuit of claim 1 wherein the reference voltage is less than or equal to about 1V.

16. (Original) The circuit of claim 1 wherein a supply voltage of the circuit is less than about 1V.

17. (Currently Amended) The circuit of claim 1 wherein [[Q1]] the first BJT device module is a pnp type and receives the output of [[CS1]] the first current source at its emitter, and wherein the second BJT device module [[Q2]] is a pnp type and receives the output of the second current source [[CS2]] at its emitter through the first resistor [[R1]].

18. (Currently Amended) The circuit of claim 1 further comprises first and second unit gain buffers setting voltages across [[R3]] the third resistor and [[R4]] the fourth resistors

by passing the outputs of the first current source [[CS1]] and the third current source [[CS3]].

19. (Currently Amended) A method for generating a temperature independent reference voltage, the method comprising:

generating first, second and third current outputs (CS1, CS2, and CS3), with the first current source [[CS1]] feeding into an emitter of a first pnp BJT device module (Q1), the second current source [[CS2]] feeding into an emitter of a second pnp BJT device module (Q2) through a first resistor ~~resister~~ (R1), and the third current source [[CS3]] connecting to a grounding voltage supply through a second resistor ~~resister~~ (R2);

providing three current paths from a current summing circuit to the ground voltage supply through third, forth and fifth ~~three~~ resistors (R3, R4, and R5) respectively;

imposing an emitter voltage of Q1 (V_{be1}) across the third resistor [[R3]];

imposing a voltage across [[R2]] the second resistor to be across the fourth resistor [[R4]],

wherein a temperature independent reference voltage (V_{REF}) across the fifth resistor [[R5]] is generated when V_{be1}, an emitter voltage of Q2 (V_{be2}), and the resistors bear a predetermined relationship as represented mathematically by $(R5 / R3) * dV_{be1}/dT + ((R2 * R5) /(R1 * R4)) * d(V_{be1} - V_{be2})/dT = 0$, wherein dV_{be1}/dT and $d(V_{be1} - V_{be2})/dT$ are respective changes of the emitter voltage of [[Q1]] the first pnp BJT device module and a difference between the emitter voltages of [[Q1]] the first pnp BJT device module and [[Q2]] the second pnp BJT device module with respect to temperature.

20. (Currently Amended) The method of claim 19 further ~~comprises~~ comprising using an operational amplifier with its negative input connected to the first current source [[CS1]] and positive input connected with the second current source [[CS2]] for maintaining a same current through the first pnp BJT device module [[Q1]] and the second pnp BJT device module [[Q2]].

21. (Currently Amended) The method of claim 19 wherein the current summing circuit provides the current through [[R5]] the fifth resistor to be proportional to the summation of the currents through the third resistor [[R3]] and the fourth resistor [[R4]].

22. (Currently Amended) The method of claim 19 wherein the reference voltage is less than or equal to about 1V.